UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SONDERMAN, BUSHMAN, and CHRISTIAN

Appeal 2007-2454
Application 09/880,975
Technology Center 2800

Decided: 28 January 2008

Before RICHARD TORCZON, SALLY GARDNER LANE, and MICHAEL P. TIERNEY *Administrative Patent Judges.*

LANE, *Administrative Patent Judge.*

DECISION ON APPEAL

I. Statement of the Case

This is a 35 U.S.C. § 134 appeal in the above-referenced case. We have jurisdiction under 35 U.S.C. § 6(b) to review the rejections of claims 1, 7-12, and 22. We affirm the rejections.

The application was filed on June 13, 2001. The real party in interest is said to be Advanced Micro Devices, Inc. (App. Br. of September 13, 2005, at 2).

The field of the claimed invention is semiconductor fabrication technology. (Spec. at 2). Specifically, the claimed invention relates to a method and a system for achieving a desired thickness of a copper layer on a semiconductor.

The following U.S. patents were relied upon by the Examiner:

Name	Patent No.	Issue Date
Ritzdorf et al.	6,428,673	Aug. 6, 2002
Ueno	6,221,765	Apr. 24, 2001
Breiner et al.	6,298,470	Oct. 2, 2001
Jun et al.	6,211,094	Apr. 3, 2001

Appellants do not dispute the prior art status of any of these references.

The following two grounds of rejection are appealed:

Claims 1, 7-12, and 22 are rejected under 35 U.S.C. § 103(a) as being obvious over Ritzdorf, in view of Ueno and Breiner.

Claims 1, 7, 8, 10, 11, and 22 are rejected under 35 U.S.C. § 103(a) as being obvious over Ritzdorf, in view of Ueno and Jun.

Appellants responded to the claims for each rejection as a group and did not present separate arguments for individual claims. *See* App. Br. of September 13, 2005, at 39; Bd. R 37(c)(1)(vii). For each ground of rejection we have selected claim 1 as a representative claim because none of the claims were argued separately by Appellants. *See In re McDaniel*, 293 F.3d 1379, 1382-83, (Fed. Cir. 2002). Claim 1 recites:

> A method comprising:
> forming a first dielectric layer above a first structure layer;
> forming a first opening in the first dielectric layer;
> forming a first copper layer above the first dielectric layer and in the first opening; and
> measuring an actual thickness of the copper layer,

measuring the actual thickness comprises averaging a plurality of thicknesses from a plurality of locations on said first copper layer;

comparing the actual thickness to a desired thickness;

measuring a mechanical stress relating to said first copper layer;

varying at least one parameter used to form the first copper layer in response to the actual thickness differing from the desired thickness and said mechanical stress.

II. Findings of Fact

Specification

1. The specification teaches that the thickness of a copper layer in semiconductor fabrication can be controlled by varying parameters such as (1) "duration that the wafer . . . remains in the electrolytic solution;" (2) "type of features present on the wafer:" (3) "voltage and/or current applied to the anode;" and (4) "frequency, magnitude, and/or shape of the AC signal." (Spec. at 21-22).

Ritzdorf

2. Ritzdorf relates to an apparatus for processing a microrelectronic workpiece (Ritzdorf at Abstract), such as a semiconductor wafer (*Id.* at col. 1, ll. 19-23).

3. Specifically, Ritzdorf teaches "the desirability of automatically adjusting a workpiece processing step to effect its output to compensate for a condition on the workpiece such as a layer thickness, to provide an output which is tuned to the requirements determined in part by the incoming material." (Ritzdorf at col. 3, ll. 23-28).

4. To achieve this automatic adjustment, Ritzdorf teaches:

> The apparatus of the invention can include a control that modifies the process parameters of a process in order to compensate for material variations in the incoming

> microelectronic workpiece, in order to produce a uniform output or desired output from the process. The material variations in the microelectronic workpiece fed to this second process could be due to variability in a prior process step or to the use of different operations or processing chambers to feed the process. The apparatus of the invention can include an in-line metrology measurement system to determine the condition of the incoming microelectronic workpiece material, and a control for altering the process conditions based on the measurement results, i.e., a feed forward control. The metrology system may additionally be used to measure the output of the process as well. Alternately, the metrology system can measure the output of the process and the control can alter the process conditions of subsequently processed microelectronic workpieces, i.e., a feed back control.

(Ritzdorf at col. 3, line 64, through col. 4, l. 15).

5. Ritzdorf teaches that thickness data is a parameter to be used in process control, by providing:

> The metrology system can be used to measure the first workpiece of a lot, or to measure from a specific process location of the prior step (e.g., a given chamber on a seed layer sputtering tool) to verify good incoming quality of seed layers or other parameters. Likewise, the metrology system can feed forward or feed back uniformity and thickness data to drive the process recipe for electroplating reactors.

(Ritzdorf at col. 4, ll. 34-41).

6. Ritzdorf also teaches that other parameters, in addition to thickness, may be measured by providing: "The microelectronic workpiece is then transported to the metrology unit in a step 508 and film thickness and/or other parameters are measured." (Ritzdorf at col. 9, ll. 52-54).

7. The teaching of Ritzdorf encompasses both damascene (Ritzdorf at col. 3, ll. 13-14) and dual damascene (Ritzdorf at col. 5, ll. 17-20) processing.

Ueno

8. Ueno relates to manufacture of a semiconductor with damascene copper interconnects. (Ueno at col. 1, ll. 25-27).

9. Ueno discusses problems encountered in damascene copper interconnects, such as void formation and less than optimal self-annealing. (Ueno at col. 1, ll. 45-52).

10. Ueno discloses that

> it may be expected that a plating film can be formed in a manner that a compressive stress is generated in the film, to allow a stress to act in a direction enhancing shrinkage of the plating film, i.e., to accelerate self-annealing. This invention is based on the idea. In the method of this invention, a plating film is formed while distorting the semiconductor substrate into a concave where the center of the surface to be plated extrudes. Thus, the plating film in which a compressive stress is generated may be formed. It may lead to reducing a self-annealing time and preventing void generation in the groove or hole.

(Ueno at col. 3, ll. 33-43).

11. The Examiner argued that one skilled in the art would have known to "measure and use for process control . . . the mechanical stress" (Ans. at 4) from the teaching of Ueno.

12. Figures 1-5 of Ueno depict

> [a]n insulating film 2 is deposited on a silicon substrate 1 and then a groove 5 is formed in a given area. Then, on the overall surface is deposited by sputtering a barrier-metal film 3 consisting of TiN e.g., 20 nm of thickness. Then, on the surface

> is deposited by sputtering a seed-metal film 4 consisting of copper for growing copper plating (FIG. 1(a)).

(Ueno at col. 7, ll. 42-47).

Breiner

13. Breiner relates to integrated circuit and semiconductor processing. (Breiner at col. 3, ll. 41-42).

14. Breiner teaches that "[e]xamples of data collected from the wafers may include, but are not limited to: . . . 2. characteristics of grown or deposited materials . . . such as thickness, ..." (Breiner at col. 4, ll. 16-23).

15. Breiner also teaches that this data may "include multiple measurements for each data point, mean values, median values, range of values, standard deviations, wafer maps of the collected data, etc." (Breiner at col. 4, ll. 60-65).

16. Breiner gives an example of a feed-forward of information in process control based on a measurement of thickness, wherein the actual thickness does not match the desired thickness. Specifically, Breiner recites:

> For instance, if a polysilicon deposition operation results in a deposition thickness of 450 Angstroms instead of a desired 500 Angstroms a number of downstream process steps may be adjusted to compensate for the variation. Thus, a subsequent process step in which the polysilicon was to be oxidized may be shortened so that an oxide grown on the polysilicon is reduced in thickness so that the resulting thickness of the polysilicon after oxidation more closely resembles the desired thickness.

(Breiner at col. 7, ll. 15-23).

17. The Examiner found, and the Appellants do not contest, that those in the art would have known that a plurality of measurements from a

plurality of locations is more reliable than measurements from one location. (Ans. at 6).

Jun

18. Jun relates to a method controlling the thickness of thin film layers in the manufacture of semiconductor devices. (Jun at Abstract).

19. Jun teaches:

> The thickness of thin films are measured at multiple measuring spots on each monitoring wafer MW1, MW2, or MW3 because the thickness varies even on a single wafer. As an example shown in FIG6, the thickness of each monitoring wafer is measured at five spots A, B, C, D, and E.

(Jun at col. 4, ll. 17-22).

20. Table 1 of Jun discloses measurements of thickness at five locations on three different monitor wafers.

21. The Examiner argued, and the Appellants do not contest, that those skilled in the art would have known that averaging a plurality of measurements from each location would provide for a more accurate process control. (Ans. at 10-11).

III. Issues

The issues are:[1]

(1) Whether Appellants have shown that the Examiner erred in rejecting claims 1, 7-12, and 22 as being obvious under 35 U.S.C. § 103, over Ritzdorf, Ueno, and Breiner.

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[1] The Examiner and Appellants have addressed the Examiner's objection to amendments of the specification. (*See, e.g.,* Reply Br. of July 3, 2006, at 4-6). Because this issue is not appealable, *see* 37 C.F.R. § 1.113, we will not consider it.

(2) Whether Appellants have shown that the Examiner erred in rejecting claims 1, 7, 8, 10, 11, and 22 as being obvious under 35 U.S.C. § 103, over Ritzdorf, Ueno, and Jun.

IV. Legal Principles

During prosecution, claims are given their broadest reasonable interpretation consistent with the specification. *In re Prater*, 415 F.2d 1393, 1404 (CCPA 1969).

To determine whether a claimed invention would have been obvious to those in the art, we look to "the scope and content of the prior art . . . ; differences between the prior art and the claims at issue . . . ; and the level of ordinary skill in the pertinent art . . . ." *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966). We limit our inquiry to these factors in this case because no evidence of secondary considerations, such as unexpected results or the failure of others, *see id.*, were presented.

In *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727 (2007), the Court recently indicated that rigid rules in the analysis of obviousness should not be used. For example, "the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim . . . ." *Id.* at 1741. Indeed, "any need or problem known in the filed of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed." *Id.* at 1742. Thus, the combination of references from different aspects of a particular art, such as semiconductor and other microelectronic workpiece processing, might be acceptable in evaluating obviousness, even if the specific objectives of the current application are not recited in the prior art patents.

V. Analysis

Thee Examiner rejected claims 1, 7-12, and 22 as being obvious under 35 U.S.C. § 103, over Ritzdorf in view of Ueno and Breiner. Appellants admit that Ritzdorf teaches a metrology system that feeds forward or feeds back uniformity and thickness data to drive a process recipe for electroplating reactors. (App. Br. of September 13, 2005, at 26); *see also* (FF 3-6). As Appellants noted, Ritzdorf does not teach measuring a mechanical stress, nor does it teach the specific steps of "forming a first dielectric layer above a first structure layer; forming a first opening in the first dielectric layer; [and] forming a first copper layer above the first dielectric layer and in the first opening." *See* App. Br. of September 13, 2005, at 26. These elements, though, are taught in Ueno.

Ueno teaches that mechanical stress is a factor that affects plating because compressive stresses generated during processing can accelerate self annealing and prevent void formation. (FF 9-10). In Ueno, the parameter of substrate shape is varied in reaction to this mechanical stress. (FF 10). The Examiner found that those of skill in the art would have known how to and would have had reason to measure a mechanical stress. (FF 11). The Appellants do not argue that one skilled in the art would have lacked the skill to or would not have had reason to measure the mechanical stress discussed in Ueno.

Because Ueno describes manufacturing damascene interconnects and problems encountered in it (FF 9), those in the art would have looked to Ueno, in combination with Ritzdorf, to find improved methods of plating. Thus, we find that the combination of Ritzdorf and Ueno teaches measuring

a mechanical stress and varying a parameter used to form the first copper layer in accordance with the mechanical stress.

Appellants argue there is no disclosure in Ueno of the importance of the mechanical stress discussed and that Ueno only "guesses" as to the effect of the stress. (*See* App. Br. of September 13, 2005, at 27). Nevertheless, we find that Ueno considered mechanical stress to be a source of concern (FF 10), and we hold that the reason why a specific quantity of mechanical stress is important is irrelevant to Appellants' claims. The claims recite only measuring a mechanical stress and varying a parameter according to that stress. No further limitations are provided. Thus, the mere acknowledgement that mechanical stress is a variable factor in damascene copper processing by Ueno, and the understanding by those in the art of how to measure and vary this stress, provides sufficient disclosure in combination with Ritzdorf.

In addition, Figures 1-5 and their description in Ueno disclose the claimed steps of "forming a first dielectric layer above a first structure layer; forming a first opening in the first dielectric layer; forming a first copper layer above the first dielectric layer and in the first opening." (FF 12). Thus, these elements of Appellants' claims were known from Ueno.

Breiner teaches collecting multiple measurements, including mean and median values, of a thickness data point for in semiconductor processing. (FF 14-16). Breiner teaches averaging only a plurality of measurements from one data point, not from a plurality of data points. However, despite Appellants' argument that Briener does not teach averaging a plurality of thicknesses from a plurality of locations (App. Br. of September 13, 2005, at 27), one skilled in the art would have had a reason to

collect a plurality of measurements from a plurality of data points, since this would provide a more reliable result. (FF 17). *In re Boesch*, 617 F.2d 272, 276 (1980 C.C.P.A.) ("discovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art."). Appellants have not argued to the contrary.

Appellants argue that Breiner does not disclose varying at least one parameter when the actual thickness differs from the desired thickness and mechanical stress (*see* App. Br. of September 13, 2005, at 27), but we have found that Ritzdorf adequately discloses using metrology data of thickness and other parameters. Because Ritzdorf and Breiner both relate to semiconductor processing (FF 2 and 13), those in the art would have looked to both references for improved processing and, thus, would have combined their teachings.

In addition, Appellants argue that Breiner teaches a "wafer map" relating to electrical responses, but not to the thickness across various portions of a semiconductor wafer. (App. Br of September 13, 2005, at 34). Even if "wafer maps of the collected data," (Breiner at col. 4, ll. 64-65) include only electrical responses, Breiner also teaches "mean values, median values, range of values, [and] standard deviations" (FF 15) that could include thickness data (FF 16). Therefore, we find that Breiner teaches measuring thickness data by averaging a plurality of thicknesses.

Jun also discloses thickness measurements from data points, including from a plurality of points, for example in Table 1. (FF 19-20). Appellants argue that Jun "does not disclose averaging the plurality of thicknesses." (App. Br. of September 13, 2005, at 27). However, we agree with the Examiner that those in the art would have known that averaging a plurality

of measurements from a plurality of locations would provide for a more accurate process control (FF 21), *See Boesch, supra.* Appellants do not argue to the contrary.

Because both Ritzdorf and Jun (FF 2 and 18) relate to thickness control in semiconductor processing, those of skill in the art would have had reason to combine the teachings of Ritzdorf and Jun to render the claimed invention obvious.

We conclude that the combination of Ritzdorf, Ueno, and either Breiner or Jun, provide all the elements claimed and would have been combined by those in the art. Since the Appellants have not shown the Examiner's conclusion of obviousness to be in error, we affirm the Examiner's rejections under 35 U.S.C. § 103(a).

VI. Order

Upon consideration of the record and for the reasons given, it is

ORDERED that the Examiner's rejection of claims 1, 7-12, and 22 under 35 U.S.C. § 103(a) as being unpatentable over Ritzdorf, in view of Ueno and Breiner is AFFIRMED; and

FURTHER ORDERED that the Examiner's rejection of claims 1, 7, 8, 10, 11, and 22 under 35 U.S.C. § 103(a) as being unpatentable over Ritzdorf, in view of Ueno and Jun is AFFIRMED.

AFFIRMED

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